REMARKS

Claims 1-22 are in the present application.

Figures 1 and 1a were objected to for having informalities therein. A replacement sheet correcting the noted informality is submitted herewith to overcome the objection of figures 1 and 1a. Accordingly, it is respectfully requested that the objection of the drawings be reconsidered and withdrawn.

Claims 6-8, 13, 15, and 17-21 were objected to for containing informalities. The informalities cited in the Office Action have each been addressed and overcome by the amendment of the subject claims 6-8, 13, 15, and 17-21 as indicated in the amendments submitted hereinabove.

Therefore, the reconsideration and withdrawal of the objections to claims 6-8, 13, 15, and 17-21 is hereby requested.

Claims 1-2, 12, 13, and 17-22 were rejected in the under 35 USC 102(e) as being anticipated by Cirit. This rejection is traversed.

It is noted that Cirit discloses a method and apparatus of generating an integrated circuit layout design. According to Cirit, there is provided an apparatus and method for generating design netlists which meet timing and performance specifications of a circuit design. (See Cirit col. 2, ln. 61-64) The Cirit disclosed method and apparatus "rely on a special cell library having the property of constant replacement delays...and preferably a relatively large, but still discrete choices of drive strengths."(emphasis added) (See Cirit col. 2, ln 66 - col. 3, ln. 3) Cirit is disclosed as addressing the "timing closure" problem of IC design. As such, Cirit discloses a method and apparatus directed to timing optimization of an IC design layout.

Regarding the timing optimization, Cirit discloses that each original cell in

the layout is replaced with a replacement cell from the constant delay library 350 which has the same replacement delay for the total load of gate capacitance and wire loads a the original cell had with the gate load only (See Cirit col. 8, ln. 57-61).

Applicant's claim 1 states, in relevant part, an automated computer-implemented method for reducing the number of distinct IC logic cells to implement an IC comprising,

> determining an implementation of said cell based on said functional description and said design constraint, wherein the number of distinct IC logic cells for implementing said IC design is reduced.

Claim 22 recites a storage media including program instructions for the method of claim 1, and is worded similar to claim 1. Clearly, Applicant claims a method and apparatus including the step of determining an implementation of the cell based on the functional description and the design constraint, wherein the number of distinct IC logic cells for implementing the IC is reduced. That is, the claimed method makes a determination based on the functional description and the design constraint that is related to a context-of-use that reduces the number of distinct logic cells for implementing the IC.

Unlike Applicant's claimed invention, Cirit does not appear to be concerned with reduction in the number of cells for implementing an IC design. Instead, Cirit is directed to methods of timing optimization for design netlists. The Cirit special library of cells having the property of constant replacement delays are not disclosed (or even suggested) as reducing the number of cells for implementing the design. In fact, Cirit discloses replacing an original cell with another cell from a family of cells having the same replacement delay as the original cell. (See Cirit, col. 48 - col. 5, ln. 19). Again, the family of replacement cells are disclosed as having constant replacement delays and preferably having a relatively large choices of drive strengths. That is, the choices for replacement

cells are relatively large, not reduced in number. Thus, there is no reduction in the number of cells to implement the particular target design according to Cirit. This is counter to Applicant's claims of reducing the number of cells for implementing the IC.

Contrary to Applicant's claimed invention, it appears that an IC design according to Cirit may even have more cells for implementing the IC than an original implementation so long as the overall delay contributed to the replacement cells is constant with the original cell.

Therefore, it is respectfully submitted that claims 1 and 22 are not anticipated by Cirit under 35 USC 102(e).

Claims 2, 12, and 13 depend from claim 1. Applicant respectfully submits that claims 2, 12, and 13 are patentable over Cirit under 35 USC 102(e) for at least the reasons stated above regarding claims 1 and 22.

Regarding claim 3, it is respectfully submitted that the claimed determining whether the functional description and the constraint can be matched by an existing cell and the matching disclosed by Cirit are not the same or even analogous to each other. According to Cirit, "match" clearly refers to a cell "electrically appropriate for the load at the output of the cell". (See Cirit, col. 8, ln. 16). This definition is consistent with match as used throughout Cirit.

Applicant discloses the claimed matching as an equivalence/compatibility of functionality and "in addition to functionality, the target for matching is annotated with constraints that preferably relate to the target design's use in a design environment." (See Specification, p. 8, ln. 27 - p.9, ln 3)

Thus, it should be clear that the matching of Cirit and the claimed matching are not the same. Cirit fails to disclose or suggest matching the

functional aspects of the replacement cells to the original cells but instead discloses matching the electrical characteristics to obtain proper delay characteristics. Accordingly, it is respectfully requested that the rejection of claim 3 under 35 USC 102(e) be reconsidered and withdrawn.

Regarding claims 17-21, it is noted that claim 17 includes the recitation of characterizing partitions of the IC design at a transistor level. Claims 18-21 depend from claim 17. Despite the Office Action's specific citation to Cirit at col. 7, ln. 45 - col. 8, ln.12, there does not appear to be any disclosure in Cirit of transistor level partitioning of the IC design. Applicant respectfully submits that Cirit does not explicitly disclose partitioning at the transistor level.

Accordingly, Applicant respectfully requests the reconsideration and withdrawal of the 35 USC 102(e) rejection of claims 1-3, 12, 13, and 17-22, as well as the allowance of claims 1-3, 12, 13, and 17-22.

Claims 4-11 and 14-16 were rejected under 35 USC 103(a) as being unpatentable over Cirit in view of Touzet. This rejection is traversed.

Regarding the rejection of claims 4, 5, 8, and 9, it is noted that the rejection relies on the alleged disclosure of all of the elements of claim 3 by Cirit. As discussed in detail above, Cirit does not disclose or suggest all of the claimed elements of claim 3 (and base claim 1). Accordingly, the citation to and reliance on secondary reference Touzet for the use of signature determination combined with Cirit fails to render Applicant's claims 4, 5, 8, and 9 obvious.

Regarding the rejection of claims 6, 7, and 14-16, it is highlighted that the rejection relies on the alleged disclosure of all of the elements of claim 1 and 12 by Cirit. As discussed in detail above, Cirit does not disclose or suggest all of the claimed elements of claims 1 and 12. Accordingly, the citation to and reliance on secondary reference Touzet for teaching determining of at least one input

permutation or one possible input complement combined with Cirit fails to render Applicant's claims 6, 7, and 14-16 obvious.

The rejection of claims 10 and 11 are traversed on the same basis as claim 4 above. Claims 10 and 11 depend on claim 9 that in turn depends from 4 that is dependent on claim 3. Claims 10 and 11 are not obvious under 35 USC over Cirit in view of Touzet at least since claims 3 and 4 are patentable over Cirit and Touzet as discussed hereinabove.

In summary, it is respectfully submitted for the reasons set forth above, that this amendment places the application in condition for allowance. Accordingly, it is respectfully requested that claims 1-22 be allowed and the application be passed to issue.

Respectfully Submitted,

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